What is claimed is:

1. A method of manufacturing a semiconductor device having a first and second transistor respectively of an electrostatic discharge protection circuit and internal circuit, the method comprising the steps of:

providing a substrate;

forming gates of the first and second transistor on the substrate;

depositing a mask layer and patterning the mask layer using one single mask to remove the mask layer on the gates, a portion of a drain region of the first transistor, and a source and drain region of the second transistor;

implementing a first ion implantation with a first concentration under the masking of the patterned mask layer;

removing the mask layer and forming sidewall spacers of the gates; and

implementing a second ion implantation with a second concentration, wherein the concentration of the second implantation is heavier than that of the first implantation.

2. The method as claimed in claim 1, wherein the first ion implantation is N^- type ESD implantation.

3. The method as claimed in claim 1, wherein the second ion implantation is N^+ type drain diffusion.

4. The method as claimed in claim 1, wherein the first ion implantation is P^- type ESD implantation.

5. The method as claimed in claim 1, wherein the second ion implantation is P^+ type drain diffusion.

6. The method as claimed in claim 1, wherein a layout structure of the first implantation is for a single MOSFET.

7. The method as claimed in claim 1, wherein a layout structure of the first implantation is for a MOSFET in a stacked configuration structure.

8. The method as claimed in claim 1, wherein a first depth of the first implantation is larger than that of the second implantation.

9. The method as claimed in claim 1 further comprising the step of:

forming interconnections so that the drain region of the first transistor is coupled to a pad, and the source region and gate of the first transistor is coupled to receive a ground voltage.

10. The method as claimed in claim 1 further comprising the step of:

forming plugs on the gate, drain region and source region of the second transistor.

11. An electrostatic discharge protection device coupled to a pad of an internal circuit comprising:

a substrate;

a gate formed on the substrate;

a source and drain region formed in the substrate and respectively on both sides of the gate, the drain region being coupled to the pad and the source region being coupled to receive a reference voltage; and

a lightly doped region formed in the substrate, and only between the gate and the drain region, having a depth greater than that of the drain region.

12. The electrostatic discharge protection device as claimed in claim 11, wherein the source and drain region are N^+ doped regions.

13. The electrostatic discharge protection device as claimed in claim 11, wherein the source and drain region are P^+ doped regions.

14. The electrostatic discharge protection device as claimed in claim 11, wherein the lightly doped region is an N^- type ESD implantation region.

15. The electrostatic discharge protection device as claimed in claim 11, wherein the lightly doped region is a P^- type ESD implantation region.

16. A semiconductor device comprising:

a substrate;

an internal circuit formed on the substrate, comprising:

a first gate formed on the substrate; and

a first source and drain region formed in the substrate and respectively on both sides of the first gate; and

an electrostatic discharge protection circuit formed on the substrate, comprising:

a second gate formed on the substrate; and

a second source and drain region formed in the substrate and respectively on both sides of the second gate; and

a first and second lightly doped region formed in the substrate, wherein the first lightly doped region surrounds the first drain region, the second lightly doped region is only disposed between the second gate and the second drain region, and the first and second lightly doped region both have a depth greater than that of the first and second drain region.

17. The semiconductor device as claimed in claim 16, wherein all the source and drain regions are N^+ doped regions.

18. The semiconductor device as claimed in claim 16, wherein all the source and drain regions are P^+ doped regions.

19. The semiconductor device as claimed in claim 16, wherein the first and second lightly doped regions are N^- type ESD implantation regions.

20. The semiconductor device as claimed in claim 16, wherein the first and second lightly doped regions are P^- type ESD implantation regions.